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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/709,325
Filing Date: April 28, 2004
Appellant(s): DEVRIES ET AL.

Frederick E. Cooperrider
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed December 26, 2006 appealing from the Office action mailed July 25, 2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,869,844	Liu	3-2005
6,329,691	Finzi	12-2001
6,815,771	Kimura	11-2004

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim 19 is rejected under 35 U.S.C. 102(e) as anticipated by Liu et al. (US 6869844), hereinafter Liu.

Regarding claim 19, Figure 1 of Liu shows an electronic apparatus comprising:

at least one electronic chip [10], comprising:

a first circuit design module having a first grid [14];

a second circuit design module having a second grid [12]; and

means [20; protective circuit] for electrically interconnecting said first grid and said second grid no later than a first metallization layer that accumulates a charge during a plasma process in a fabrication of said chip.

Note that "no later that a first metallization layer of said chip" and "a plasma processing" are a process designation, and would thus not carry patentable weight in this claim drawn to a product. See *In re Thorp,* 227 USPQ 964 (Fed. Cir. 1985).

In addition, there is no charge accumulation in the device of Liu in Figure 1 during a plasma process in the fabrication since a protective circuit [20] is formed (col. 3, lines 26-37).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-6 and 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Liu in view of Finzi (US 6,329,691).

Regarding claim 1, Figure 1 of Liu shows an electronic chip, comprising:

a first circuit design module having a first grid [14]; and

a second circuit design module having a second grid [12],

wherein said first grid and said second grid are interconnected in a fabrication layer.

Figure 1 of Liu shows most aspects of the instant invention except a scheme wherein two grids do not accumulates an excessive voltage due to the plasma process. Fig. 3 of Finzi shows a protection circuit wherein two grids do not accumulates an excessive voltage due to the plasma process (col. 3, line 65-col. 4, line 21).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Finzi into the device of Liu in order to have a protection circuit wherein two grids do not accumulates an excessive voltage due to the plasma process to improve a data speed.

Note that "no later that a first metallization layer of said chip" and "a plasma processing" are a process designation, and would thus not carry patentable weight in this claim drawn to a product. See *In re Thorp,* 227 USPQ 964 (Fed. Cir. 1985).

In addition, there is no charge accumulation in the device of Liu in Figure 1 during a plasma process in the fabrication since a protective circuit [20] is formed (col. 3, lines 26-37).

Regarding claim 2, Figure 1 of Liu shows at least one of said first grid and said second grid comprises a metallization grid (metal interconnect; col. 1, line 50).

Regarding claim 3, Figure 1 of Liu shows said first grid and said second grid comprise one of a power grid and a ground grid (Note that the interconnection lines form the circuits 12, 14 are connected to a source and a drain).

Regarding claim 4, Figure 1 of Liu shows said first grid and said second grid are interconnected by at least one of: a diffusion region [source/drain]; a gate of a field effect transistor; a source of a field effect transistor connected to said first grid and a drain of said field effect transistor connected to said second grid; a local interconnect; and a first metallization layer that is designed to electrically interconnect at a boundary of said first circuit design module and said second circuit design module.

Regarding claim 5, Figure 1 of Liu shows that first grid and said second grid are conductive during said plasma processing because of the charge accumulation and is nonconductive during an operation of said chip unless activated by a signal because of a protective circuit [20].

Regarding claim 6, insofar as understood, Figure 1 of Liu shows that said chip components/interconnect is fabricated in a layer that has substantially no leakage of carriers to a substrate of said chip because of the protective circuit.

Regarding claim 8, it is obvious that Figure 1 of Liu shows that said layer is temporarily activated by said plasma processing (because of the charge accumulation) such that carriers in said layer are migratable during said plasma processing (before the formation of the protective circuit).

Regarding claim 9, it is obvious that Figure 1 of Liu shows that at least one of said first grid and said second grid comprises a metal grid that includes a predetermined surface area of at least one of said first circuit design module and said second circuit design module.

Regarding claim 10, Figure 1 of Liu shows an electronic chip fabricated in accordance with claim 1 (memory chip in computer; col. 1, lines 12-13).

Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Liu in view of Kimura (US 6,815,771).

Regarding claim 20, Liu shows most aspect of the instant invention except "said chip includes a silicon on insulator (SOI) structure." Fig. 12 of Kimura shows a chip includes a silicon on insulator (SOI) structure (col. 1, lines 12-15).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Kimura into the device of Liu in order to have said chip including a silicon on insulator (SOI) structure to alleviate the problem of breakdown voltage.

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Liu in view of Finzi as applied to claim 6 above, and further in view of Kimura (US 6,815,771).

Regarding claim 7, the combined teachings of Liu and Finzi show most aspects of the instant invention except "said chip includes a silicon on insulator (SOI) structure." Fig. 12 of Kimura shows a chip includes a silicon on insulator (SOI) structure (col. 1, lines 12-15).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Kimura into the device of Liu/Finzi in order to have

said chip including a silicon on insulator (SOI) structure to alleviate the problem of breakdown voltage.

(10) Response to Argument

IN GENERAL

Starting on page 6 through page 7 of the Appeal brief, Appellants state that "... in the Advisory Action ... Examiner alleges: '*Applicants argue on page 8 that the instant invention has distinction over the prior art over the prior art with the emphasis underlined. However, these aspects are not recited explicitly in the claims.*' " Appellants' response is followed in detail to show that "the Examiner simply ignores the plain meaning of the claim language." It is, however, pointed out that the detailed arguments are not pertinent to the Examiner's statement of "*these aspects are not recited explicitly in the claims.*"

Appellants argue that "[a]s explained in paragraph [0037], the present invention teaches that the damage to the chip components is due to two-dimensional differences in charging during the plasma process, so that, as shown in figure 2, different surfaces of the chip will receive different amount of charges." However, this argument is not persuasive. In addition, it is deemed confusing. Before addressing the response to the argument, it is pointed out that the present invention is directed to solve a problem of the charge accumulation on metal layers caused during plasma processing. And in response, it is pointed out that paragraph [0037] and Figure 2 of the instant invention do not teach what is stated above in the argument. That is, the damage to the chip during the plasma

processing is not intended in order that "different surfaces of the chip will receive different amount of charges." Rather, the paragraph and the figure address a problem in a conventional device since the charge on metal layers of the conventional device differs due to the inherent occurrence of the difference in charging during the plasma processing. In other word, there is differential charge accumulation on the metal layers of the conventional device during the plasma processing. It is further pointed out that one of ordinary skill in the art readily understands that the charges accumulate on the metal layers during the device fabrication, therefore, requiring protection from the damage caused by the charge accumulation on the metal layer. (See Liu et al. in column 3, lines 7-17).

Appellants argue that "[m]oreover, as explained in paragraph [0032] and illustrated in Figure 3, the present invention exemplarily defined by independent claim 19 is directed toward a chip 300 that has a plurality of grids resultant from respective design efforts of different engineering teams." This argument is not persuasive. It is noted that claim 19 does not recite this aspect at all. At best, claim 19 recites two grids and means for electrically interconnecting the two grids. For the sake of argument, assume that the claim recites the limitation "a plurality of grids resultant from respective design efforts of different engineering teams." This recitation merely implies that there are a plurality of grids, in this case, two grids. However, note that "resultant from respective design efforts of different engineering teams" would not carry patentable weight since the final device can has the same structure as the one recited in the instant invention even though the two grids are resultant from the design efforts of the same or single engineering team. In

addition, it is further pointed out that the instant invention explicitly discloses in paragraph [0032] that it is customary that different portions of the integrated circuits are designed by different engineering teams. Therefore, a chip having "a plurality of grids resultant from respective design efforts of different engineering teams" is not a novel innovation.

On the same page of the Appeal brief, Appellants further present the arguments of "the present invention teaches that, to overcome the damage done by this unequal distribution of charges, the different grids of different design modules should be electrically interconnected before the first plasma operation after the grid has been formed." This argument is not persuasive. The instant invention does not recite that "different grids of different design modules should be electrically interconnected before the first plasma operation." Rather, the pending claims recite an electrical interconnection of two grids no later than a first metallization layer that accumulates a charge.

Therefore, it is noted that the arguments on these page of the Appeal brief do not address the supporting grounds to reverse the issue of "*these aspects are not recited explicitly in the claims.*"

GROUND 1

On page 8 of the Appeal brief, Appellants argue that "[p]rimary reference Liu does not address chips having circuits isolated from the substrate, such as SOI." Note

that the rejection is made under 35 U.S.C. 103 and the Kimura reference is introduced to complement the deficiency of SOI in the Liu reference.

Appellants argues that "[t]here is no indication in Liu of a 'first circuit design module' and a 'second circuit design module', as this terminology is discussed and described in paragraph [0032] of the disclosure. This terminology in the claims refers to the different portions of a circuit designed by different engineering teams as clearly illustrated in Figure 3." Note that the instant invention does not recite that a first and a second circuit design modules are "the different portions of a circuit designed by different engineering teams." Therefore, a 'first circuit design module' and a 'second circuit design module' merely imply a first circuit (integrated circuit) and a second circuit (integrated circuit) and Liu clearly shows a first circuit (14) and a second circuit (12). And even if a first and a second circuit design modules are intended to indicate "the different portions of a circuit designed by different engineering teams," it is noted that "the different portions of a circuit designed by different engineering teams" is not patentable novelty. As discussed in the rebuttal above, the final device could have the same configuration as the one recited in the instant invention even though the different portions of two circuit modules (circuits) are formed by the design efforts of the same or single engineering team. Furthermore, the instant invention explicitly discloses in paragraph [0032] that it is *customary* that different portions of the integrated circuits are designed by different engineering teams. (Emphasis added.)

Continuing to page 9 of Appeal brief, Appellants further argue that "... relative to claim 19, even if the line of gates shown in Figure 2 of Liu were to be considered a

'grid', the primary reference still fails to satisfy the plain meaning of the claim language, since the only protective mechanism in Liu is to the substrate and involves only the single grid. There is no mechanism that protects against a differential accumulation of charges across two grids that are isolated from the substrate, since the mechanism in Liu will inherently discharge to the substrate before a differential charge between the grid builds up. Nor is there any suggestion to provide an interconnection between two design modules." This argument is not persuasive. Note that the instant invention discloses that a grid is merely a metal line, therefore, a line formed between the gate electrode and a word line 13 in Figure 2 of Liu is a grid. And it is further noted that the instant invention does not recite a "mechanism that protects against a differential accumulation of charges across two grids that are isolated from the substrate." Rather, claim 19 merely recites the limitation "means for electrically interconnecting said first grid and said second grid no later than a first metallization layer that accumulates a charge during a plasma process in a fabrication of said chip." It is clear that this recitation does not indicate that there is a different amount of charge accumulation between the two grids. Note that the process designations "no later than" and "during a plasma process in a fabrication of said chip" would not carry patentable weight in this claim drawn to a product. With this interpretation, this limitation implies that means (a protection circuit) electrically connects the first and the second grids (metal lines) when a first metallization layer is formed with a charge accumulation. Fig. 2 of Liu shows means (20; a protection circuit) accommodates electrical connection of the first grid (a metal line connected to a source) and the second grid (a metal line connected to a gate electrode) through the connection to the first metallization

layer (13; word line). The first grid (a metal line connected to a source) and the second grid (a metal line connected to a gate electrode) are electrically connected since the source and the gate are electrical terminals of the single transistor. Liu also discloses a first metallization layer (word line) that accumulates a charge (col. 3, lines 7-17).

Appellants argue with quoting of MPEP §2173.01 that patentable weight is given to the limitation "no later than" and "during a plasma process in a fabrication of said chip" since "the finished product includes two or more grids, readily observable by one of skill in the art as indicative of a design module, and these grids will be electrically interconnected with an actual structure that will be observable by one of ordinary skill in the art." Note that Figures 2 and 3 of Liu shows all of these aspects also. That is, a finished product (10) of Liu includes two or more grids (metal lines connected to the design modules/circuits 12, 14, 15) and these grids will be electrically interconnected with an actual structure (computer, microprocessor; col. 1, lines 12-14).

On page 10 of the Appeal brief, Appellants argue that "[t]o one having ordinary skill in the art, the structure interconnecting two grids of two design modules is readily determinable as having been fabricated in a step prior to one in which a plasma processing might be used." Note that the instant invention does not recite that the interconnection is performed. Rather, the pending claims recite that the two grids are connected "no later than a first metallization layer that accumulates a charge." This recitation does not necessarily imply that the connection of the two grids is performed before the first metallization layer. This can be read that the two grids are connected

when the first metallization layer is formed, thus charge is being accumulated on it. Detailed response regarding this issue is addressed previously.

Appellants repeat the argument regarding the limitation designating the process. The core of the argument is substantially identical to the one stated on page 9 of the Appeal brief. And the rebuttal regarding this subject matter has been discussed above.

In the last paragraph on page 10 of the Appeal brief, Appellants present an argument regarding claim 19. However, note that substantially identical argument is presented on pages 8 through 9, and the corresponding rebuttal has been stated above.

GROUND 2

On page 11 of the Appeal brief, Appellants argue that "Liu has not been demonstrated as resultant from two design modules, as clearly required by the plain meaning of the claim language, and only one of the two 'grids' identified in the rejection has a protection mechanism. There is no electrical interconnection between the two grids." Note that this argument is substantially identical in nature to the one on pages 8 through 9, and the rebuttal has been made accordingly.

Appellants further argue that "[t]he Examiner further alleges that one having ordinary skill in the art would have been motivated to modify Liu by Finzi '... *in order to have a protection circuit wherein two grids do not accumulates (sic) an excessive voltage due to the plasma process to improve a data speed.*" Appellants submit that, to one having ordinary skill in the art, this rationale is a *non-sequitur* since there is no logical connection between data speed and installing another protection circuit in primary

reference Liu. Therefore, Appellants submit that this rejection fails to provide a motivation to modify the primary reference and, thus, fails to meet the initial burden of a *prima facie* rejection for obviousness." However, this argument is not persuasive. Note that the protection circuit in the Finzi's device is to alleviate the problem caused by differential charge accumulation on two grids. Therefore, this protection circuit of Finzi would replace the protection circuit in the Liu's device, not adding to the Liu's the protection circuit when the two grids have a differential charge accumulation.

On pages 11 through 12, Appellants' further contention on claim 1 has been rebutted previously since the contention is substantially identical in nature presented on pages 8 through 9.

On page 12, Appellants argue that "there will inherently be substantial leakage of current in Liu." This argument is not persuasive since Liu discloses in column 3, lines 14-17 that the word line provides a leakage path. Note that the protection circuit in the Liu's device functions in the identical manner to the one disclosed in the instant invention.

On page 12, Appellants argument on claim 9 has been addressed in the office action above.

GROUND 3

On page 13 of the Appeal brief, Appellants argue that "... Appellants submit that modification of Liu to convert it into SOI would change the underlying principle of operation of its protective mechanism, since this mechanism requires a path to the

substrate, and SOI would preclude such path. Therefore, such conversion would be improper since it would defeat the purpose of the mechanism in the primary reference. " This argument is not persuasive. As stated above, Liu discloses that the word line 13 provides a leakage path. Furthermore, the instant invention of SOI also shows that a protective mechanism (a diffusion layer 505) requires a path to the substrate.

GROUND 4

Appellant's argument is substantially identical in nature to the one presented in GROUND 3 and the rebuttal has been made above.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

JMI

Conferees:

David Blum

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